



1/31

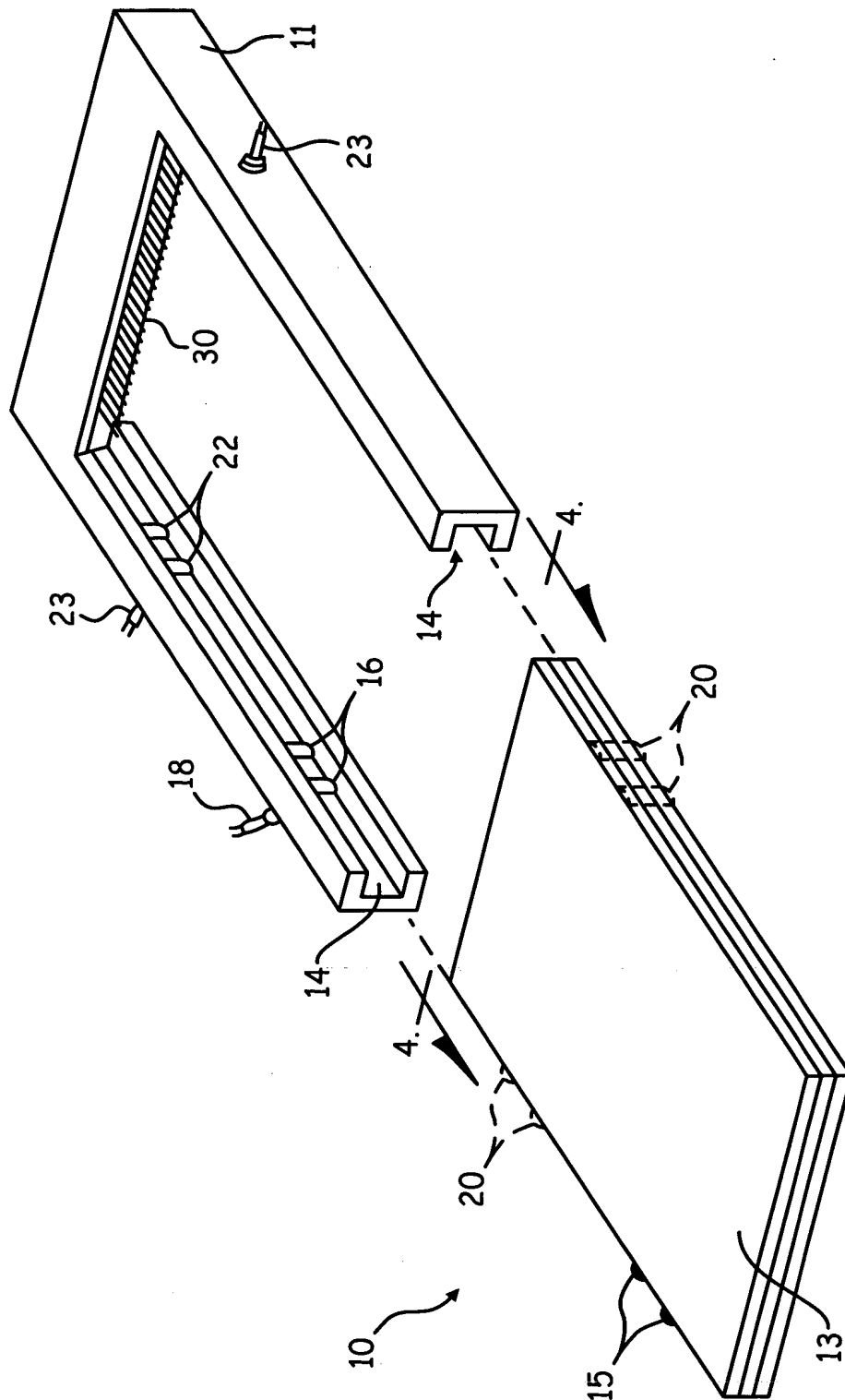


FIG. 1



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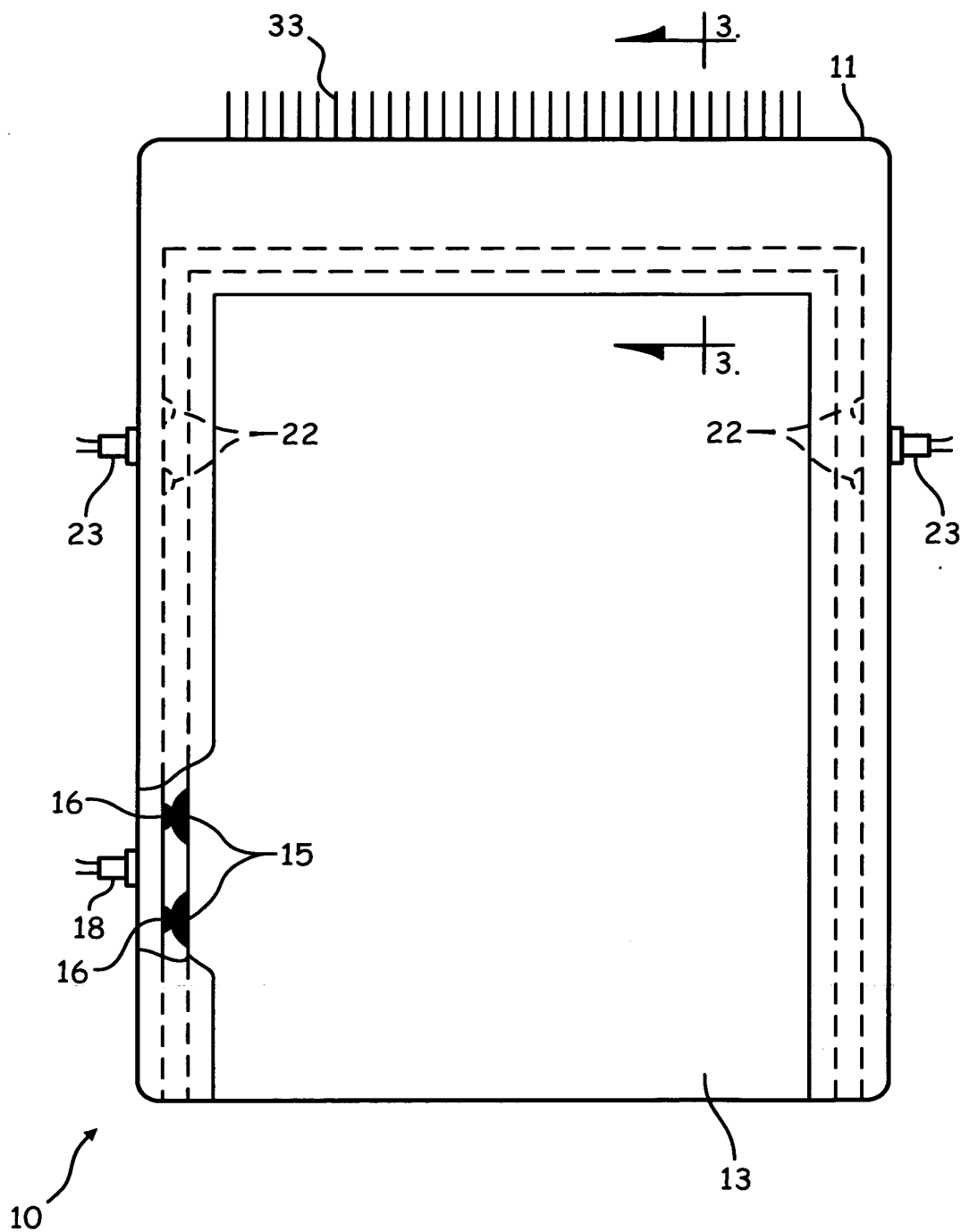


FIG. 2



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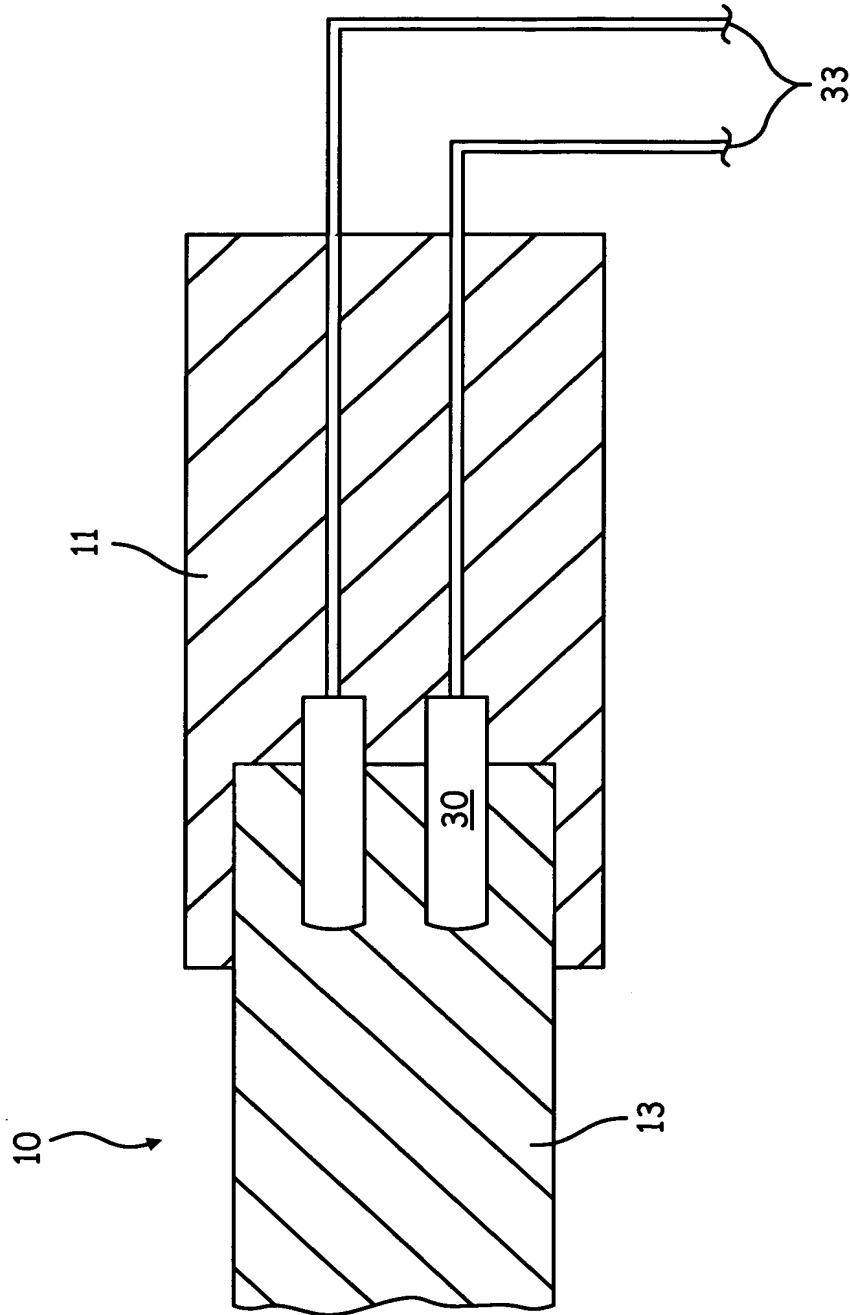


FIG. 3



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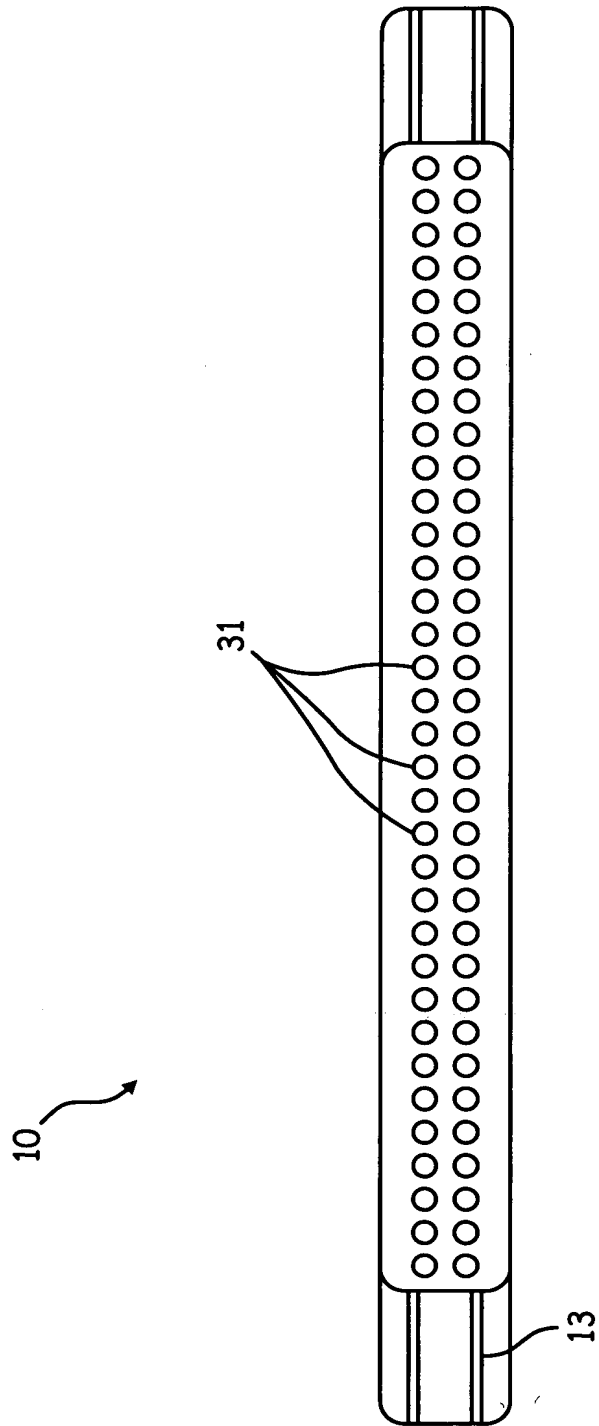


FIG. 4



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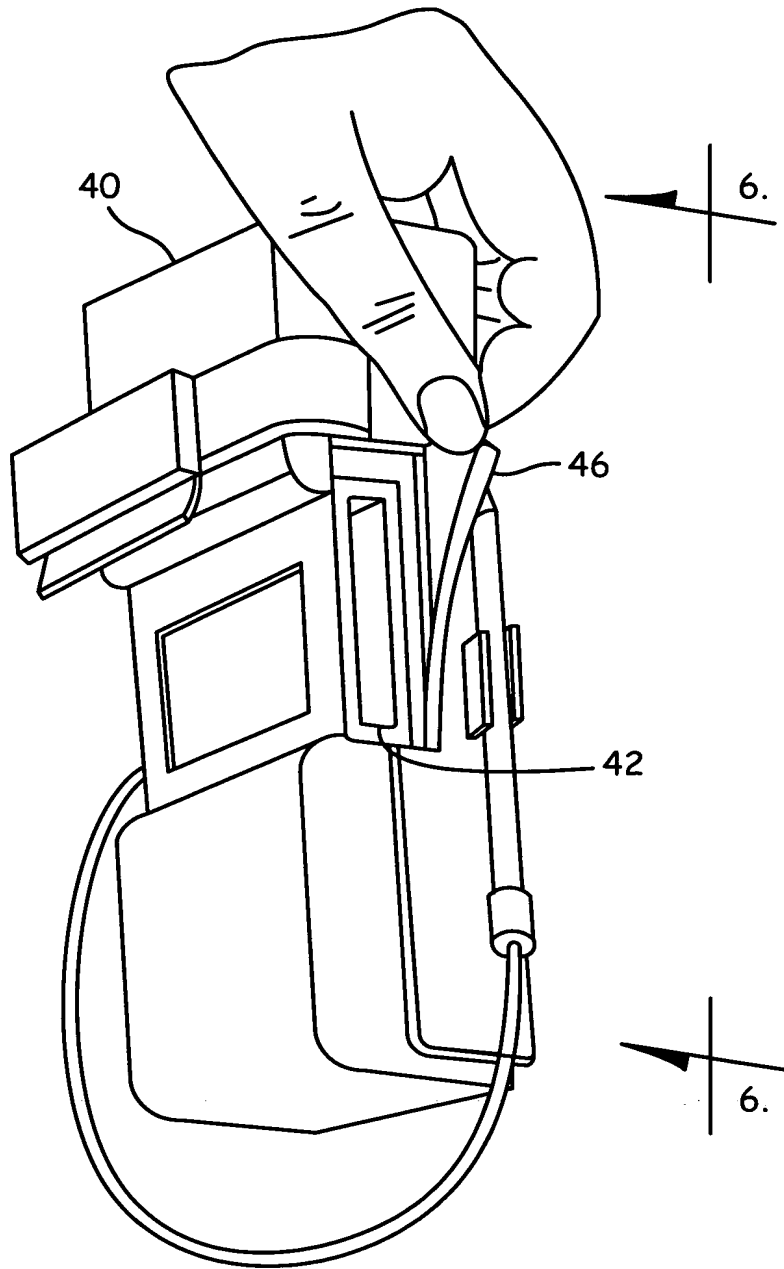


FIG. 5



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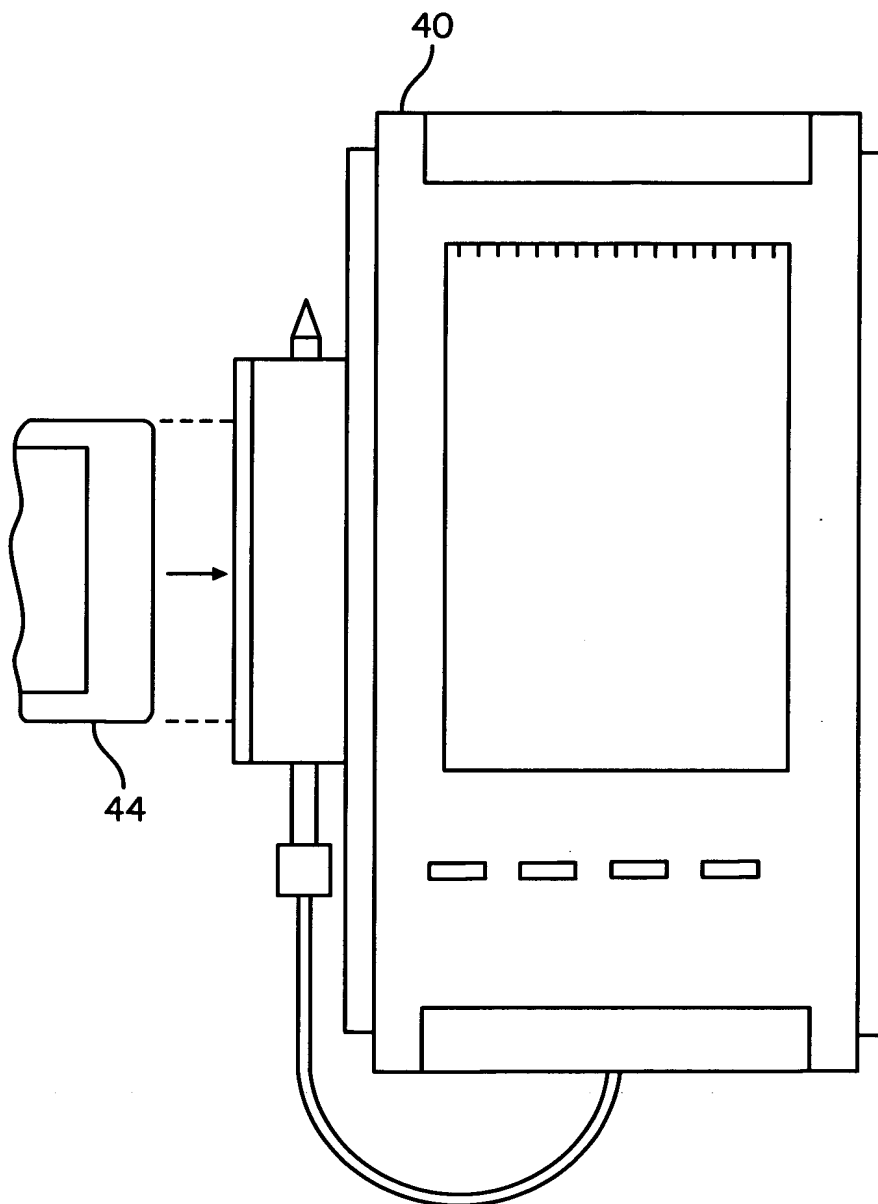
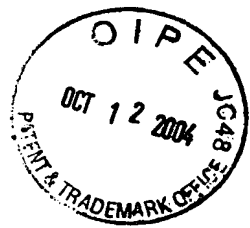


FIG. 6



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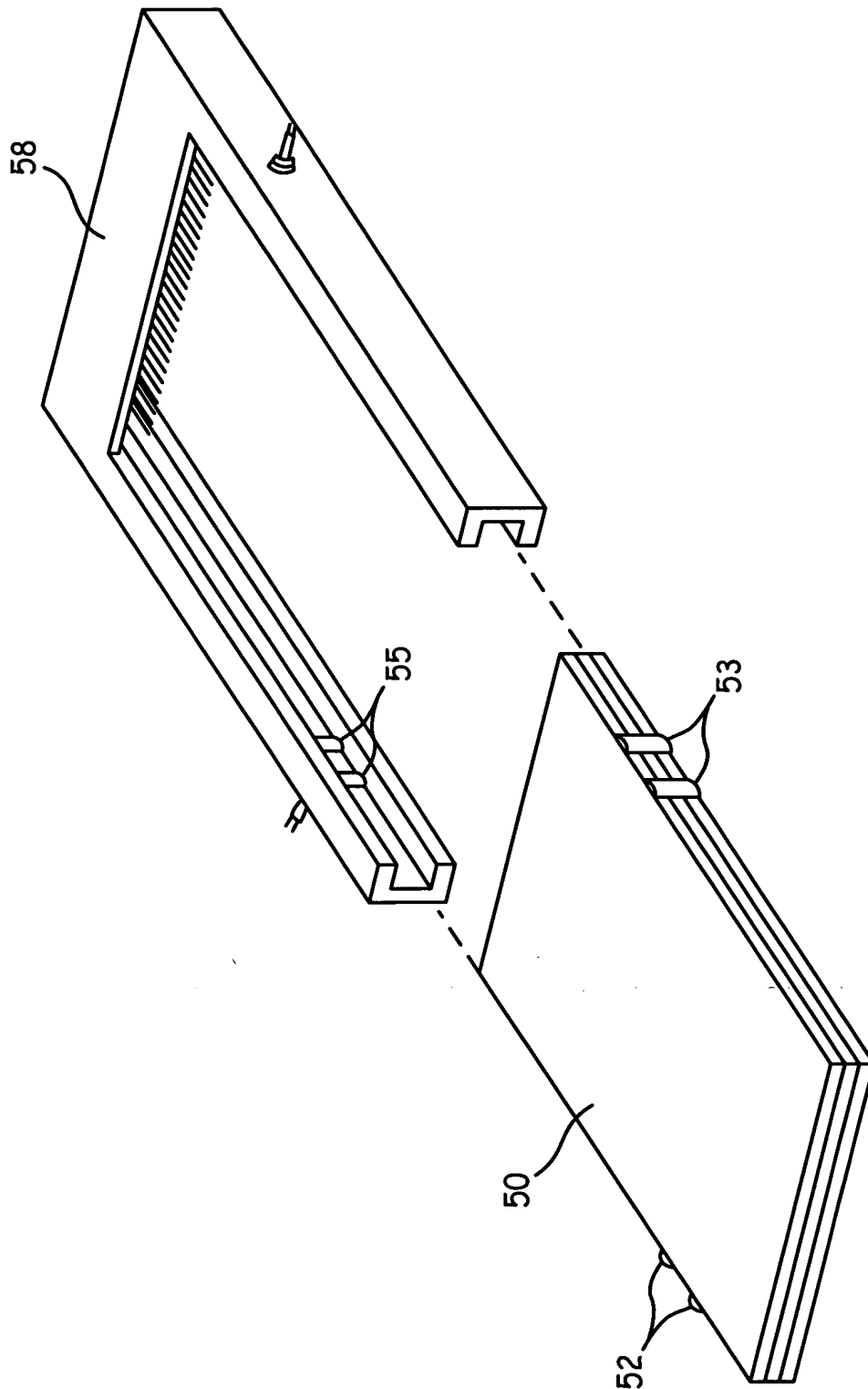


FIG. 7

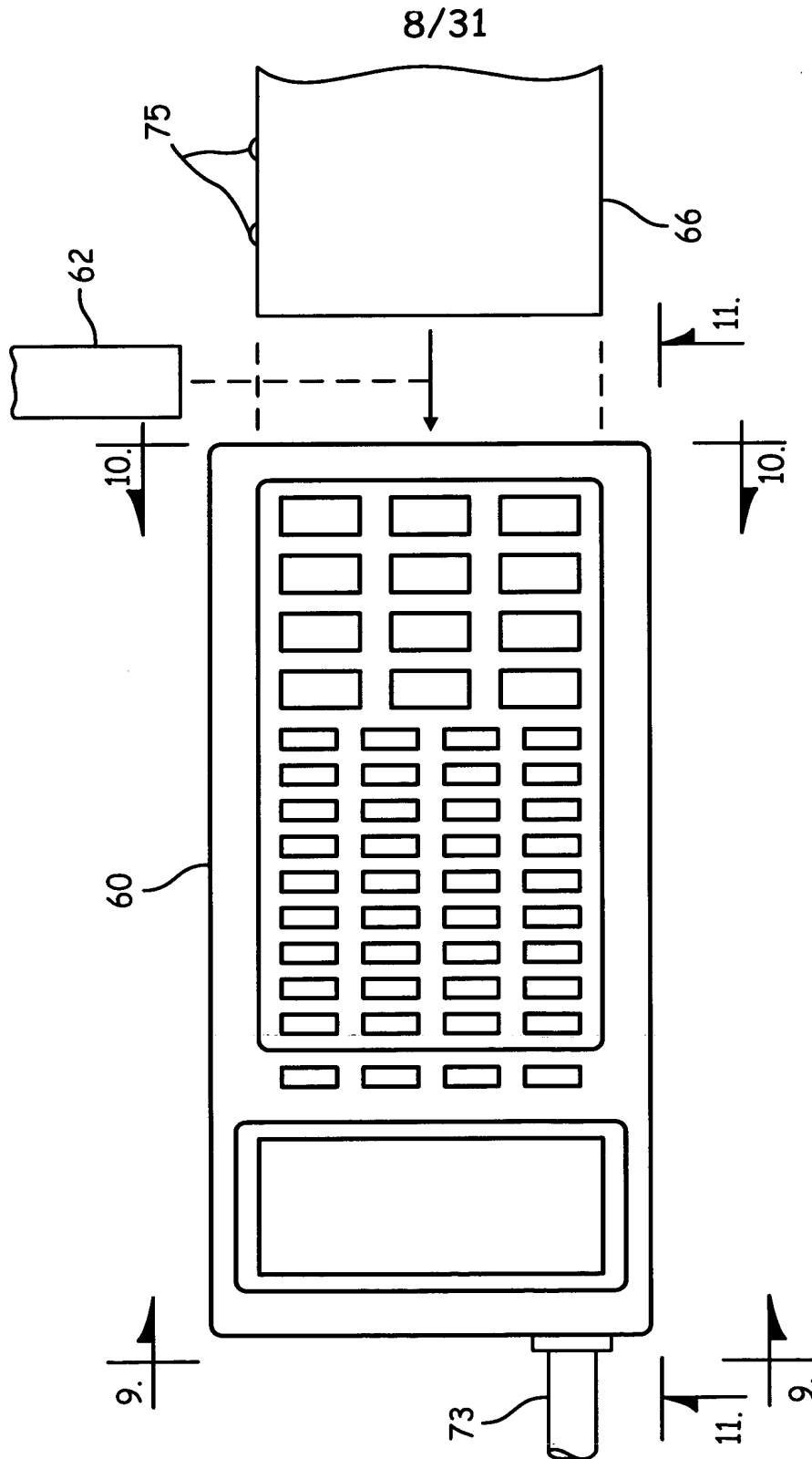
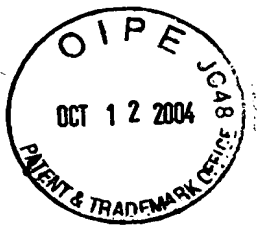


FIG. 8





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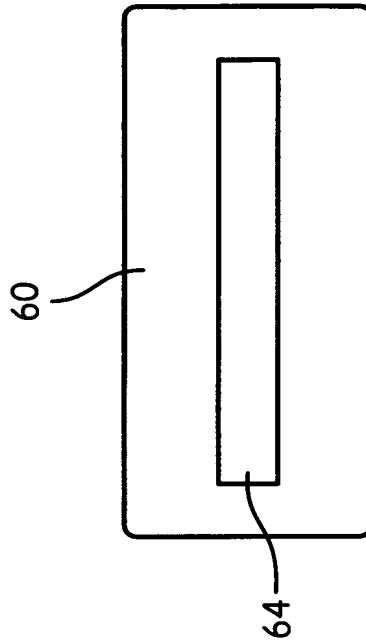


FIG. 10

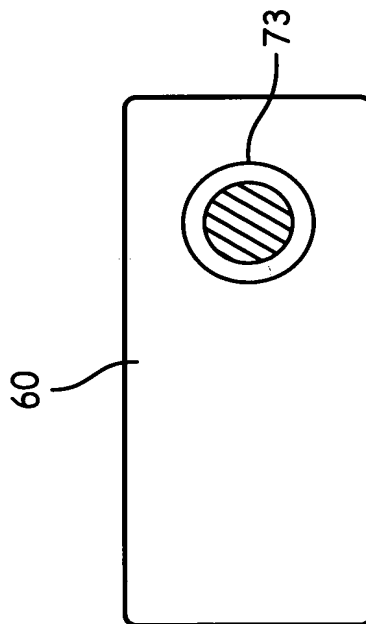


FIG. 9



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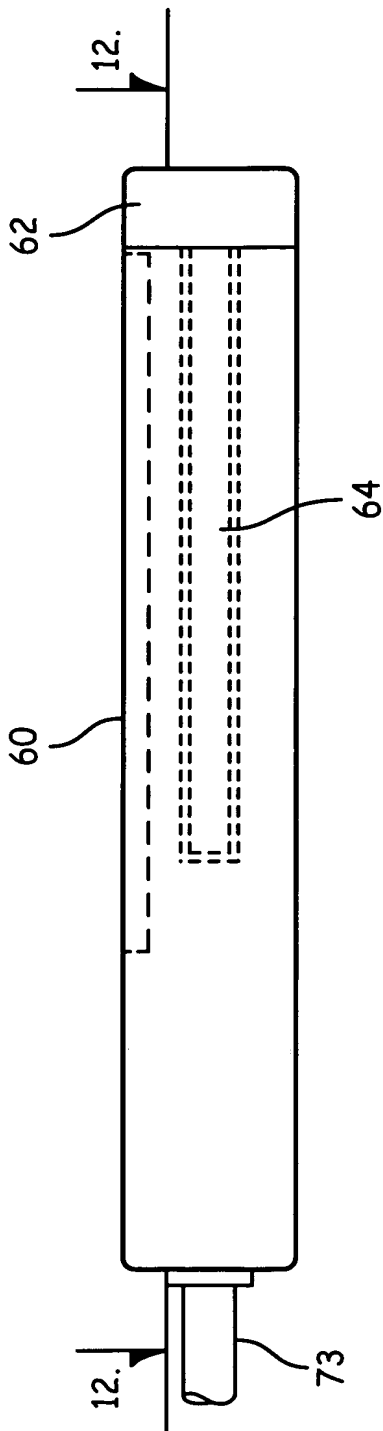


FIG. 11

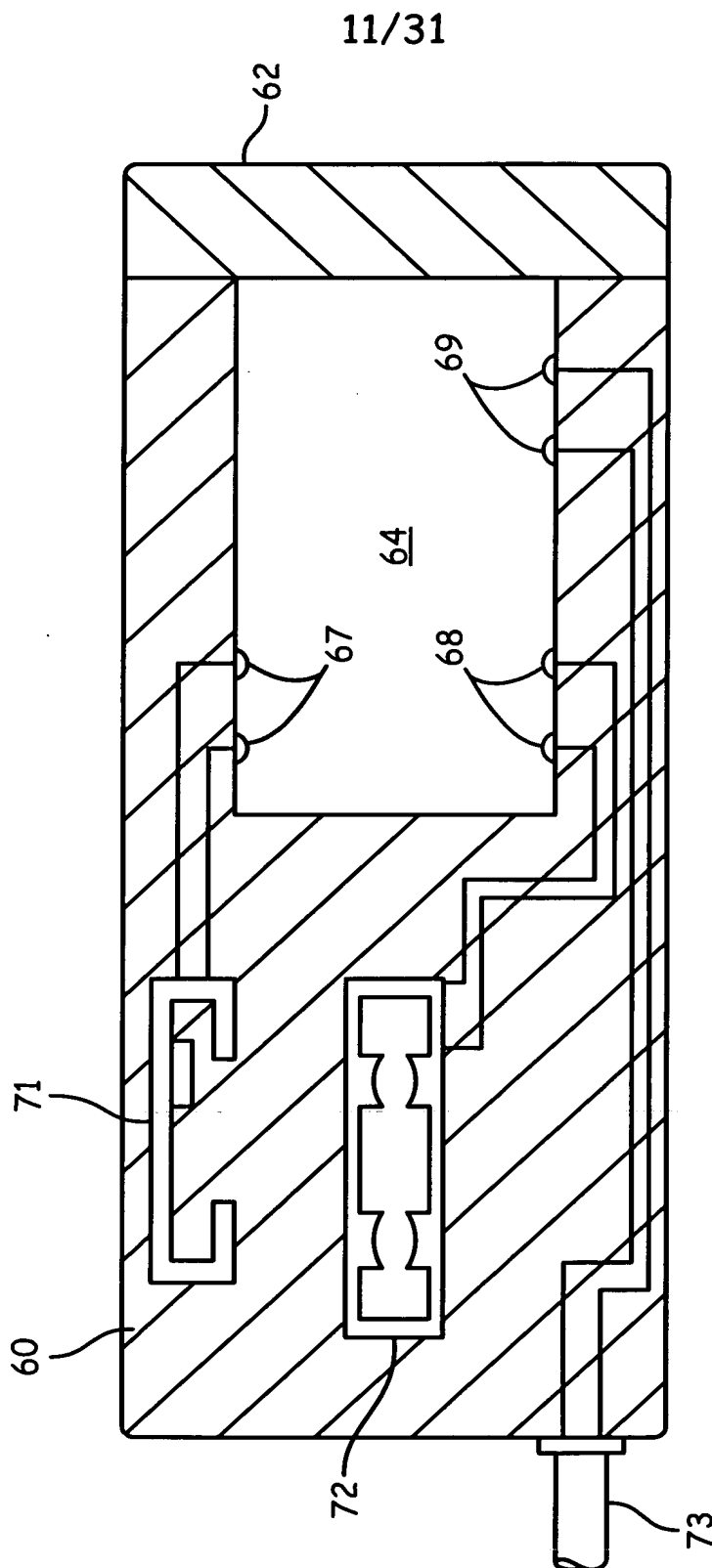


FIG. 12



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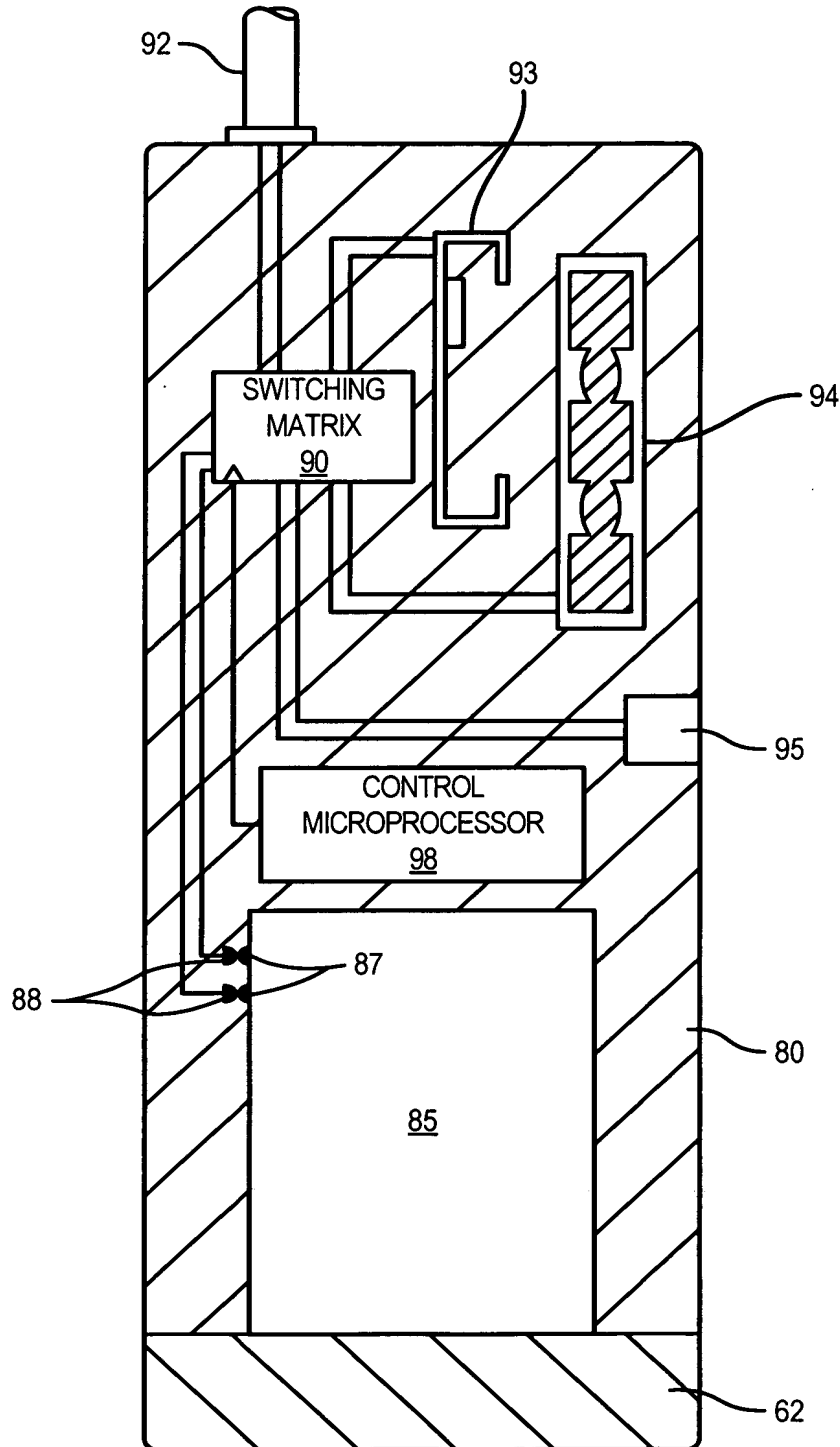


FIG. 13

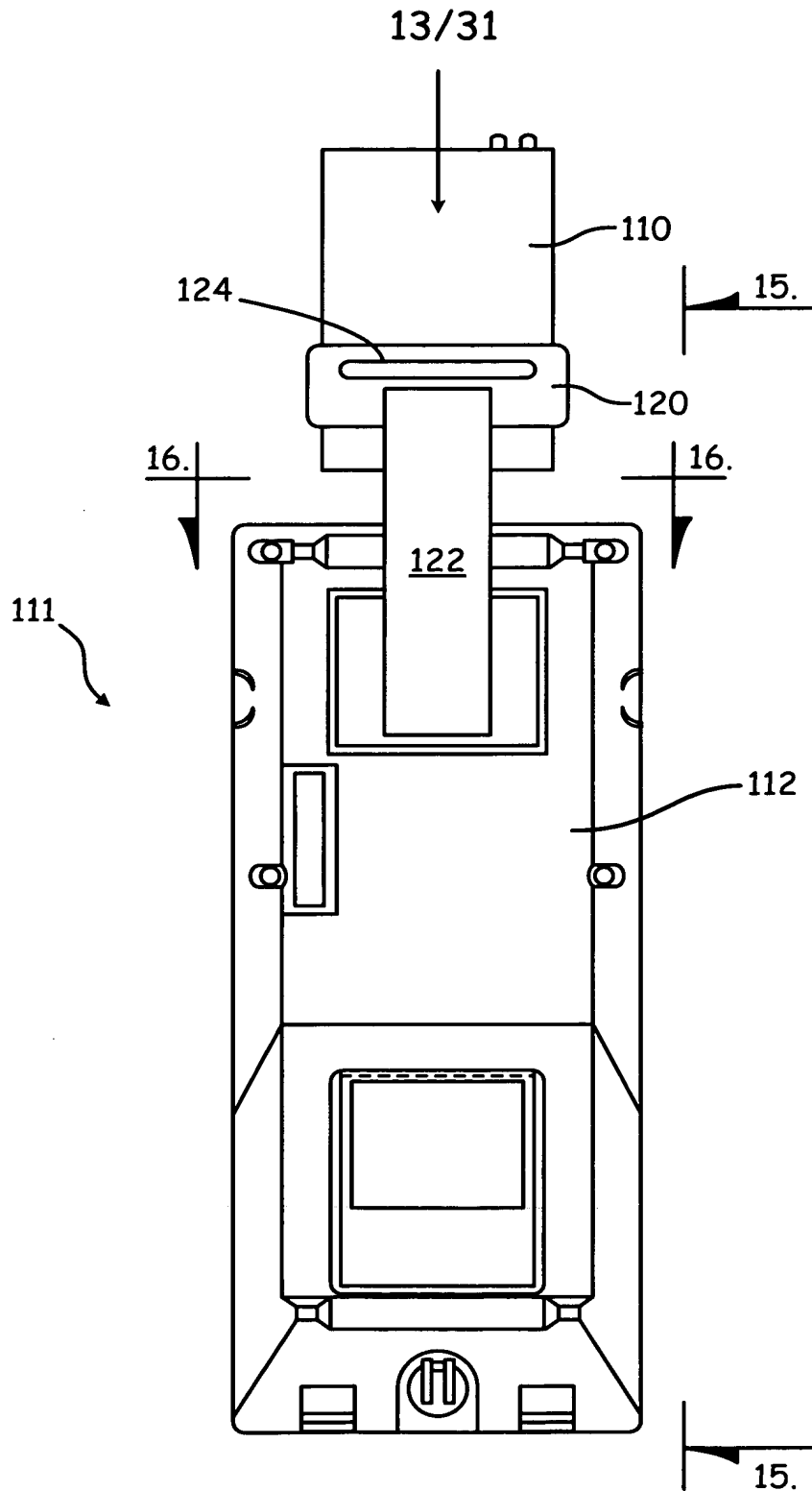


FIG. 14

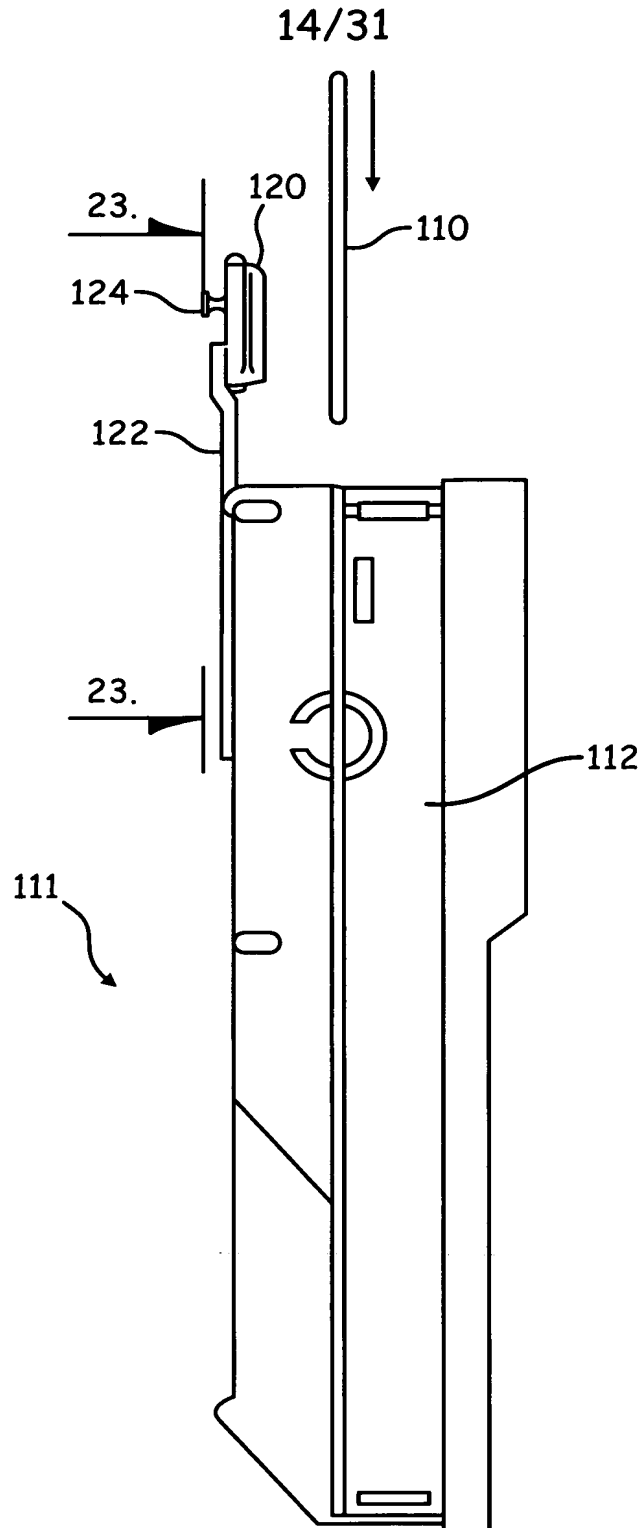


FIG. 15



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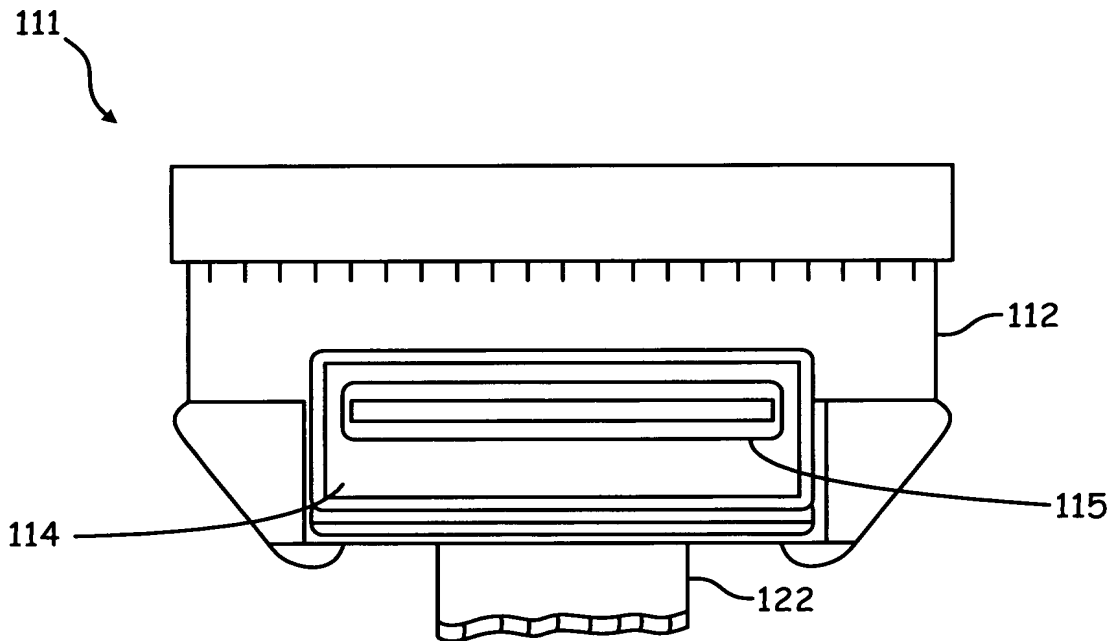


FIG. 16



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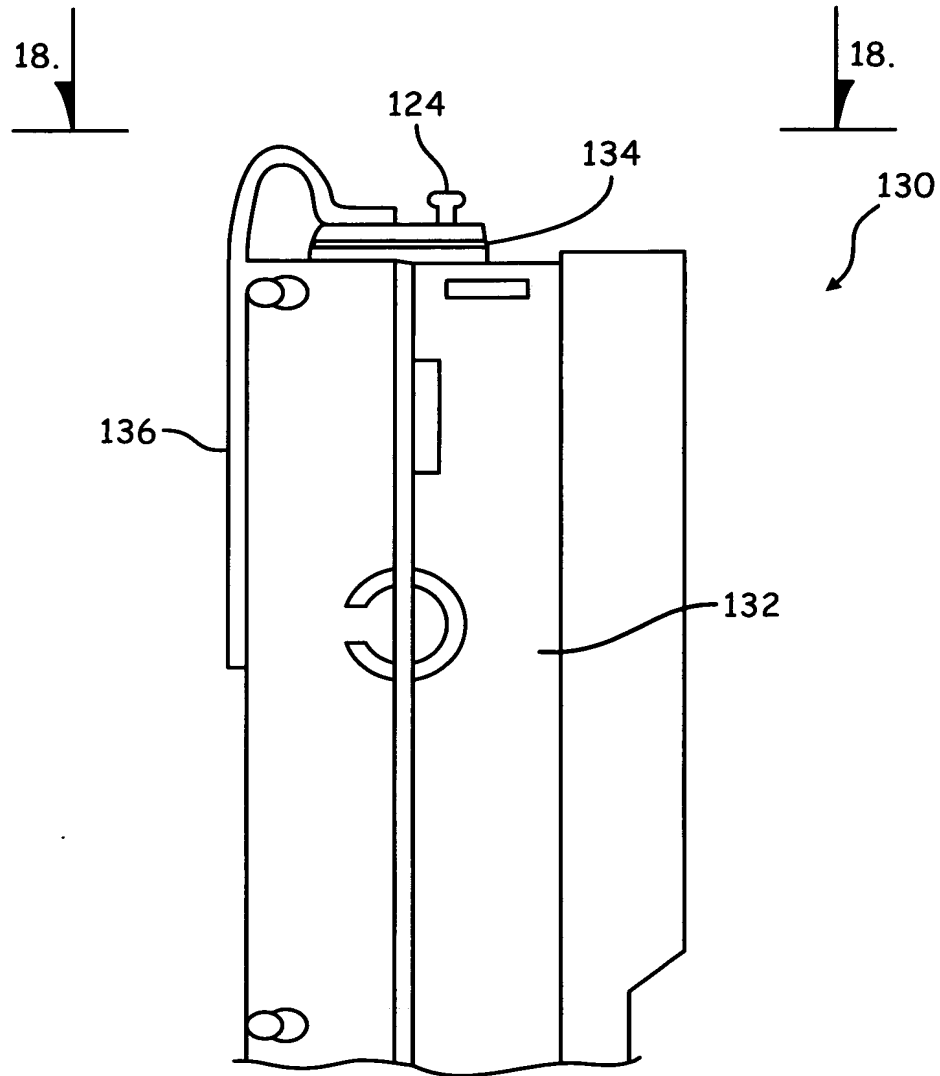


FIG. 17





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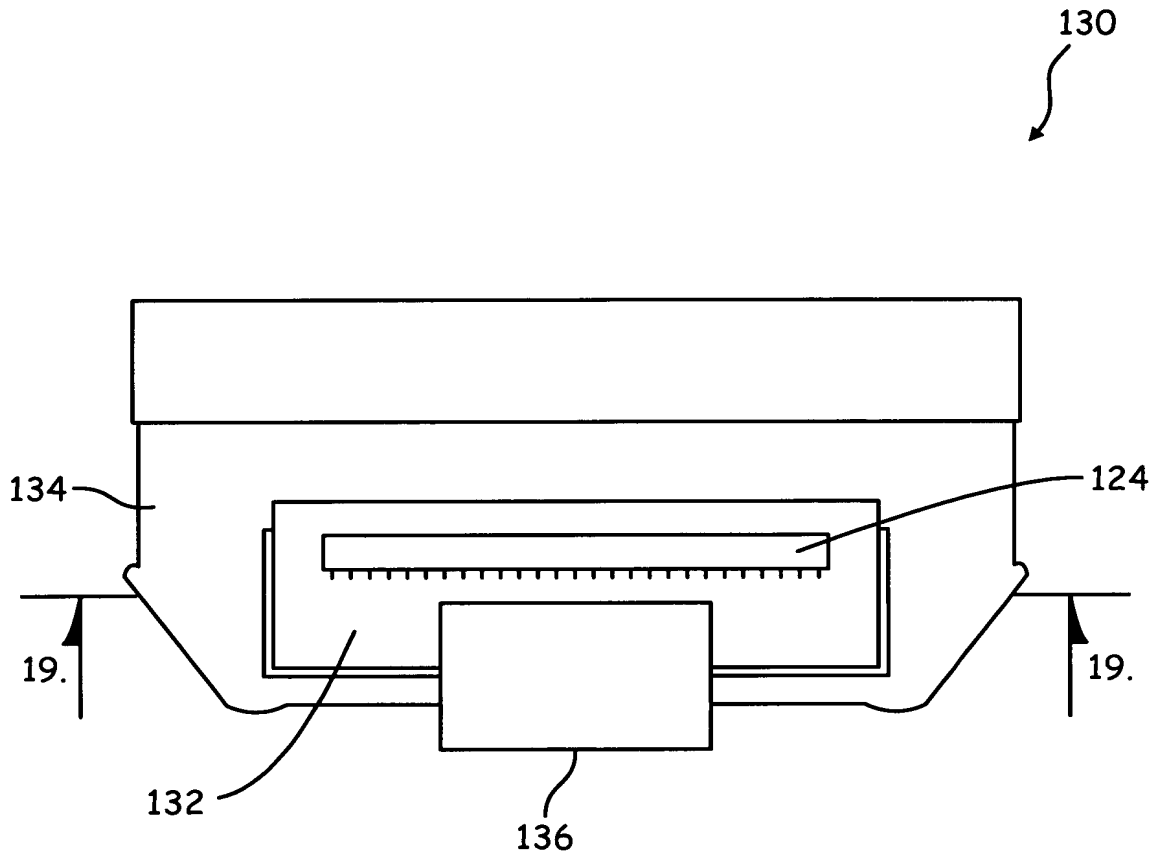
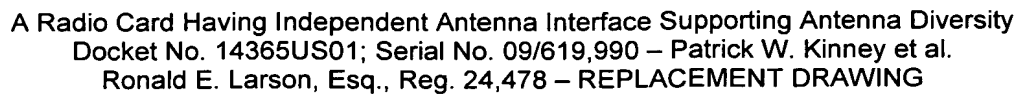


FIG. 18



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A cross-sectional view of a semiconductor device 130. The device features a substrate 132 with a central channel 134. A gate stack 135 is positioned on top of the channel 134. A source/drain region 136 is located on the left side of the channel 134. A contact 137 is formed on the top surface of the source/drain region 136. A passivation layer 138 is formed on the top surface of the device. A trench 139 is formed in the passivation layer 138, exposing the contact 137. A conductive plug 140 is formed in the trench 139, making electrical contact with the contact 137. A gate electrode 141 is formed on the top surface of the gate stack 135. A gate insulating layer 142 is formed on the top surface of the gate stack 135. A gate contact 143 is formed on the top surface of the gate stack 135. A gate insulating layer 144 is formed on the top surface of the gate stack 135. A gate contact 145 is formed on the top surface of the gate stack 135. A gate insulating layer 146 is formed on the top surface of the gate stack 135. A gate contact 147 is formed on the top surface of the gate stack 135.

FIG. 20



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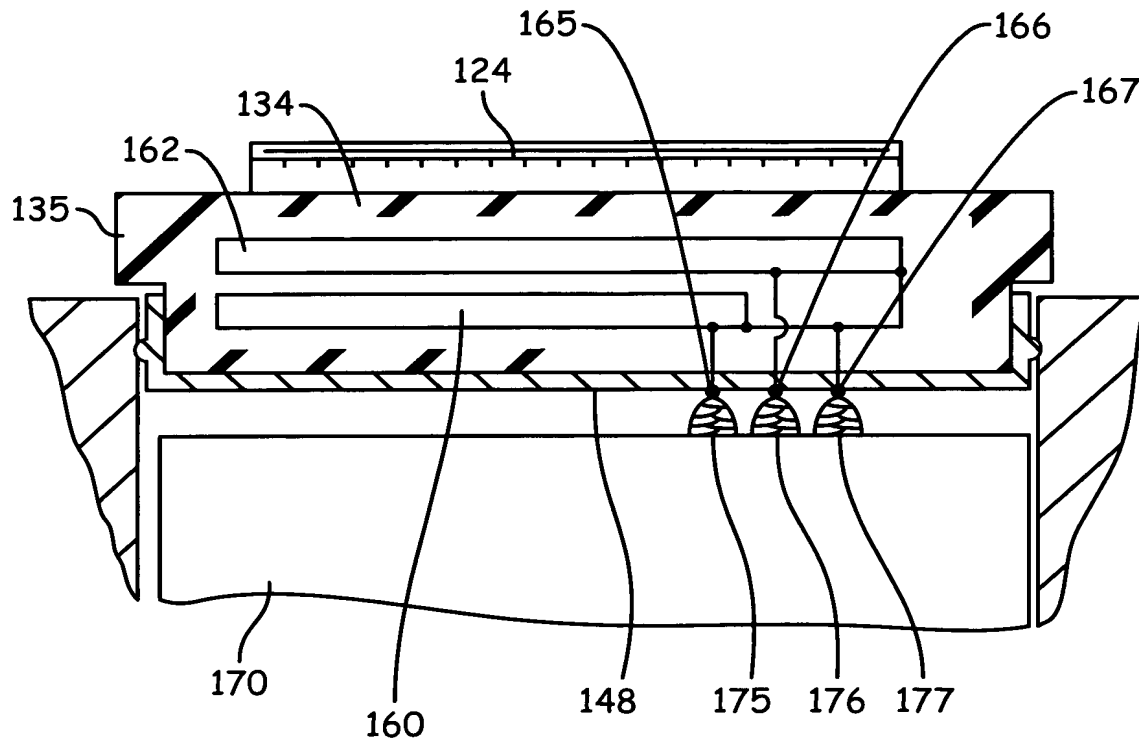


FIG. 21



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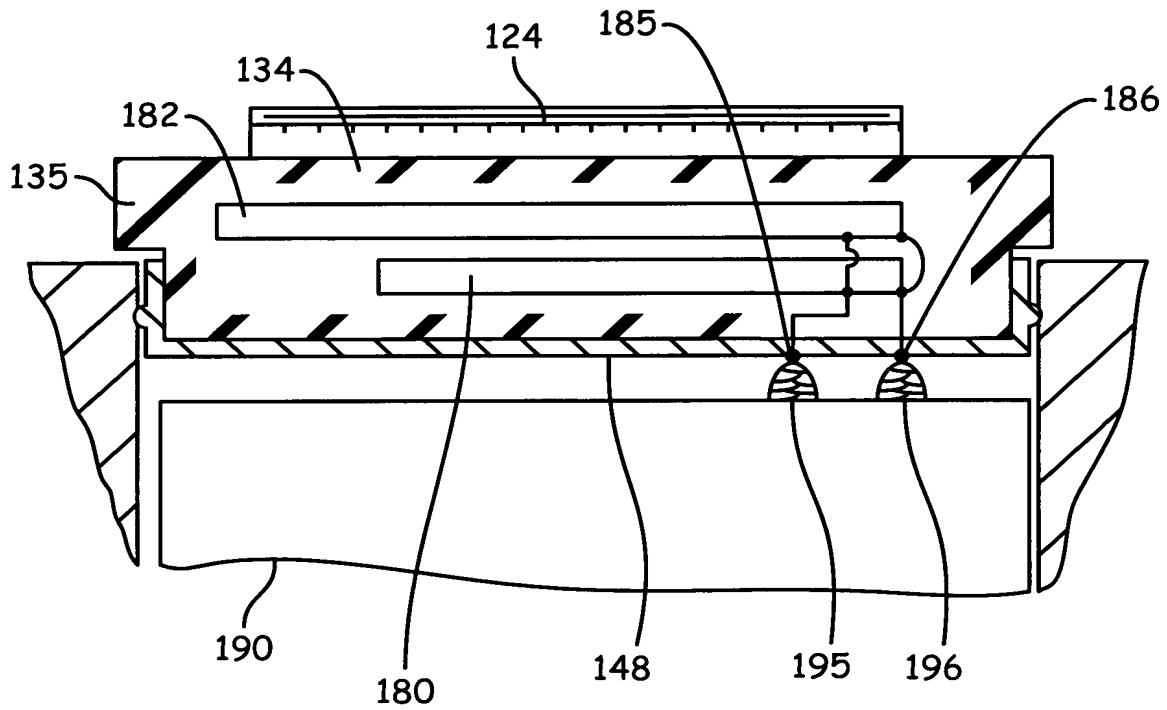


FIG. 22



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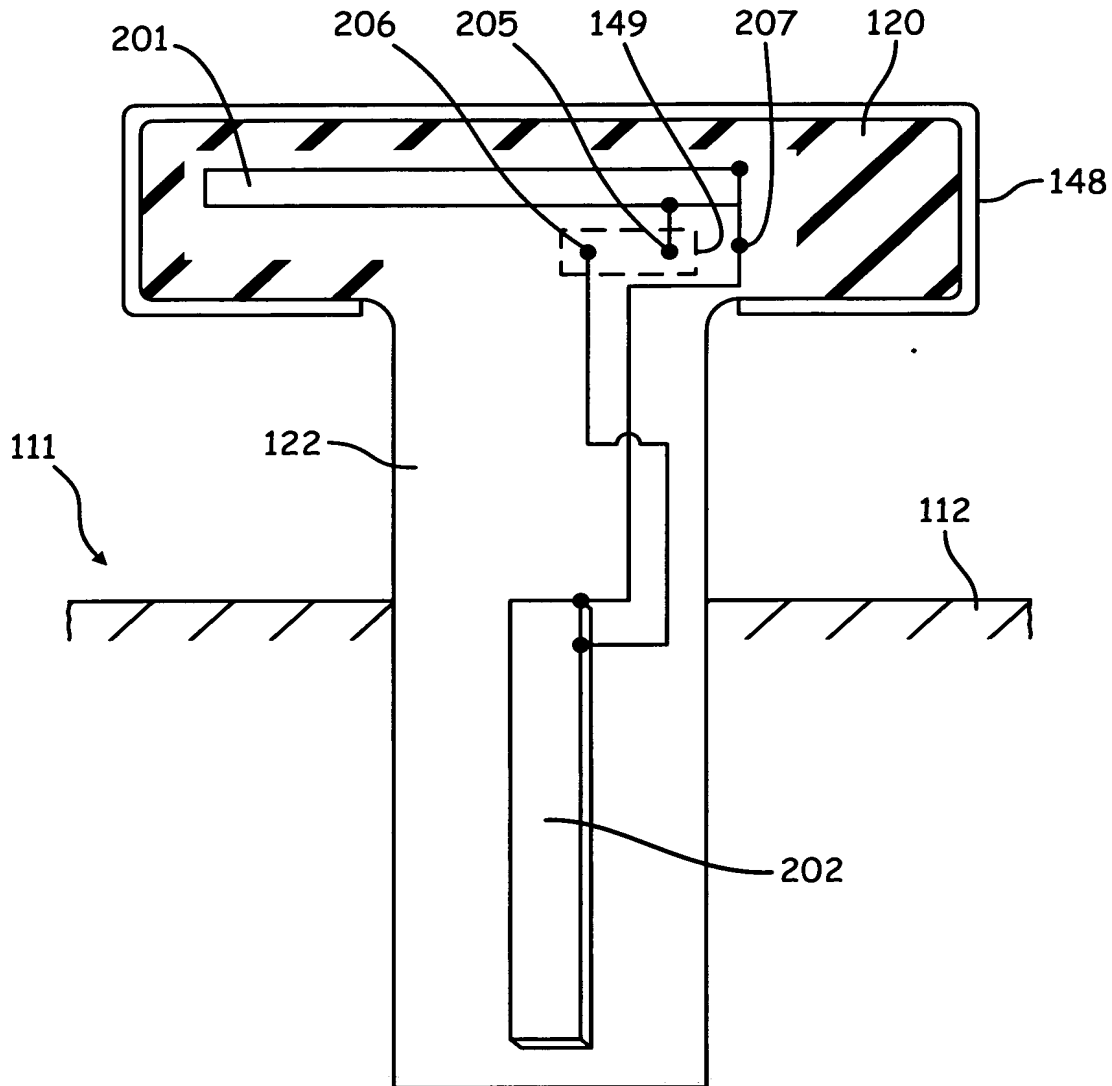


FIG. 23

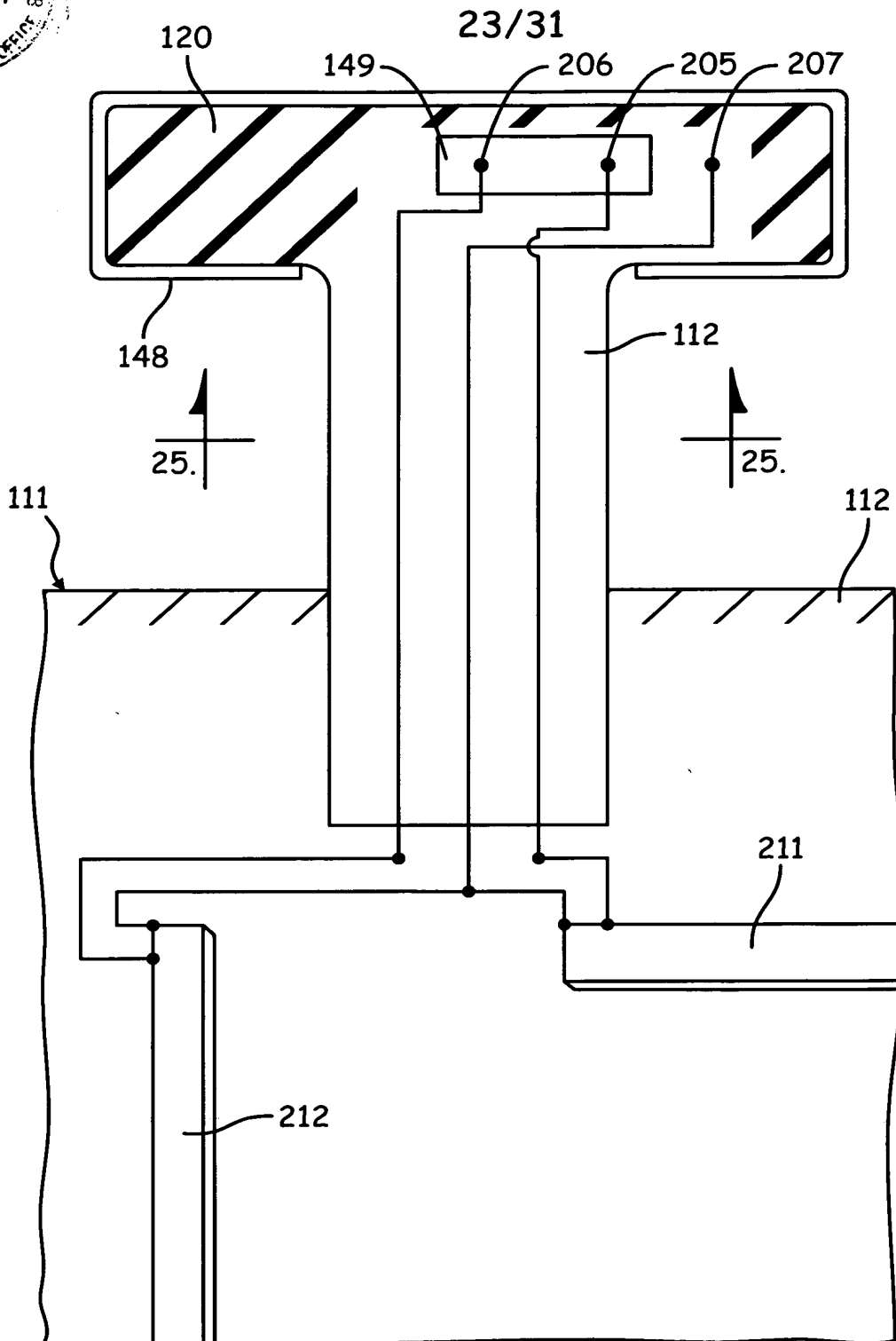


FIG. 24



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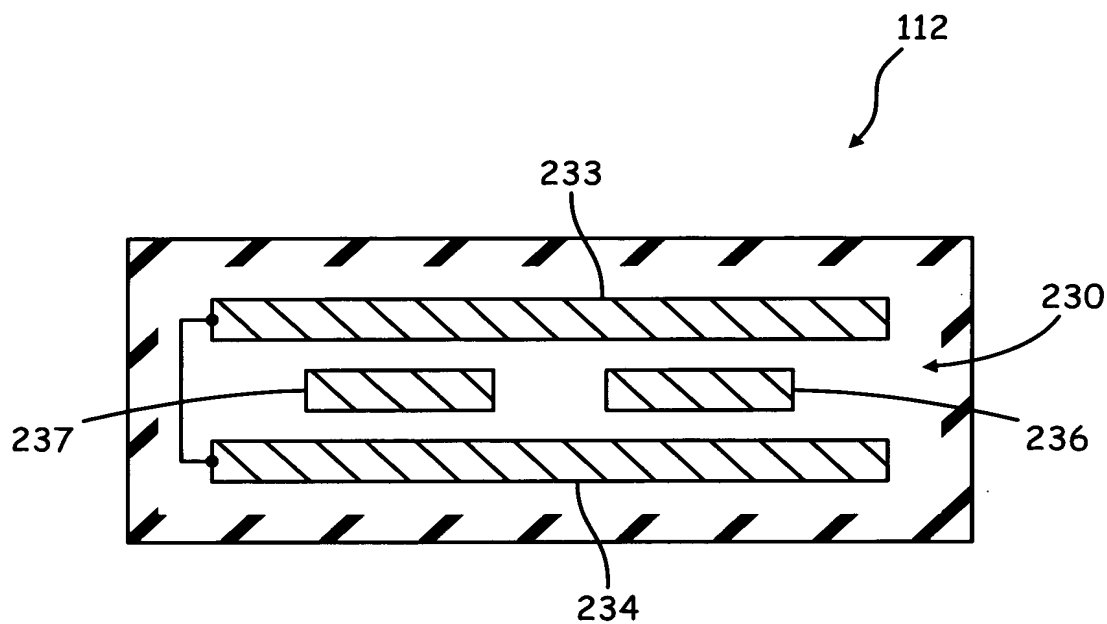


FIG. 25



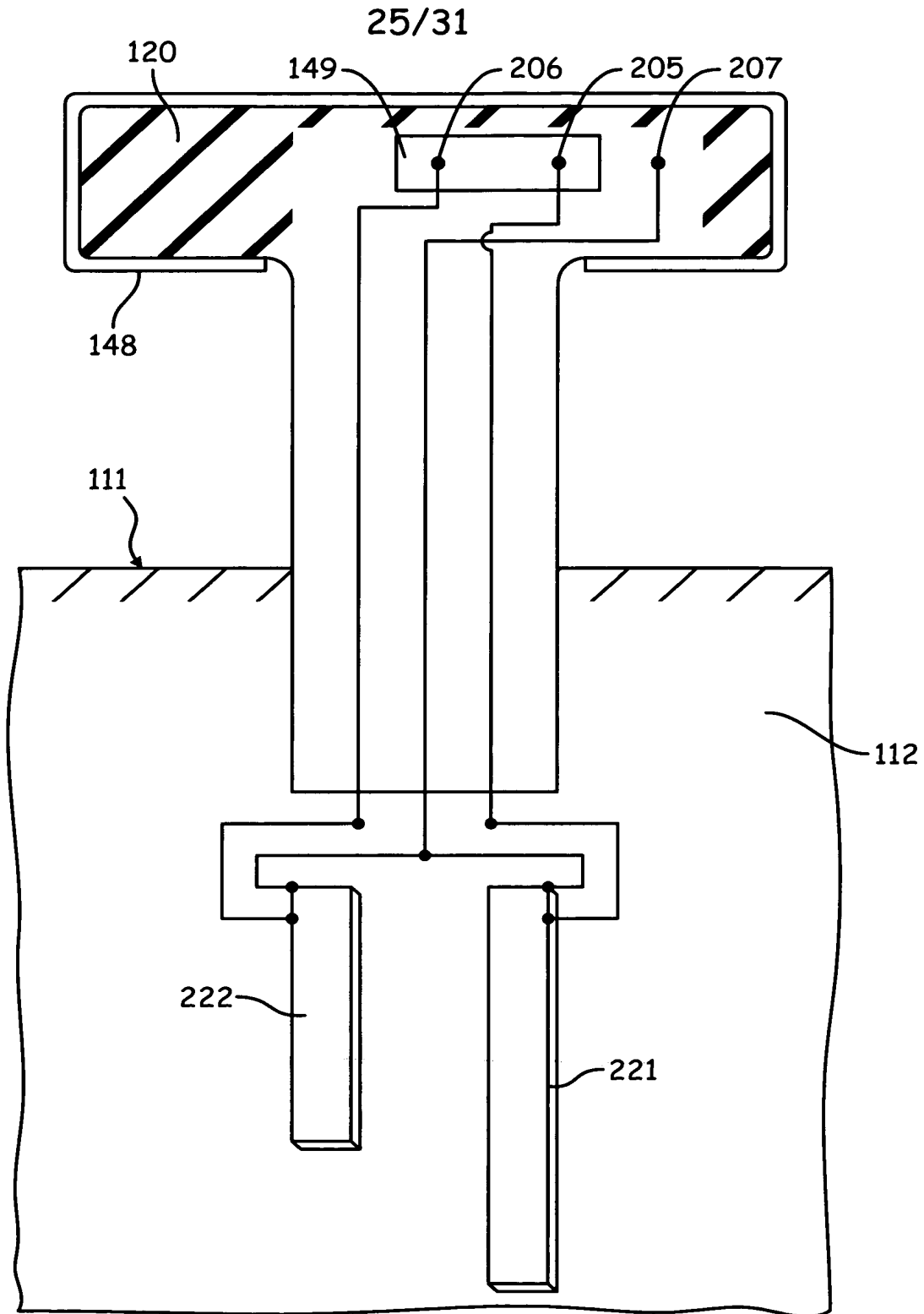


FIG. 26

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FIG. 27

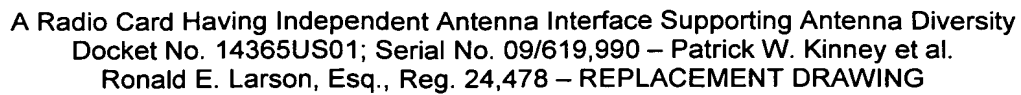
[illegible]

FIG. 28



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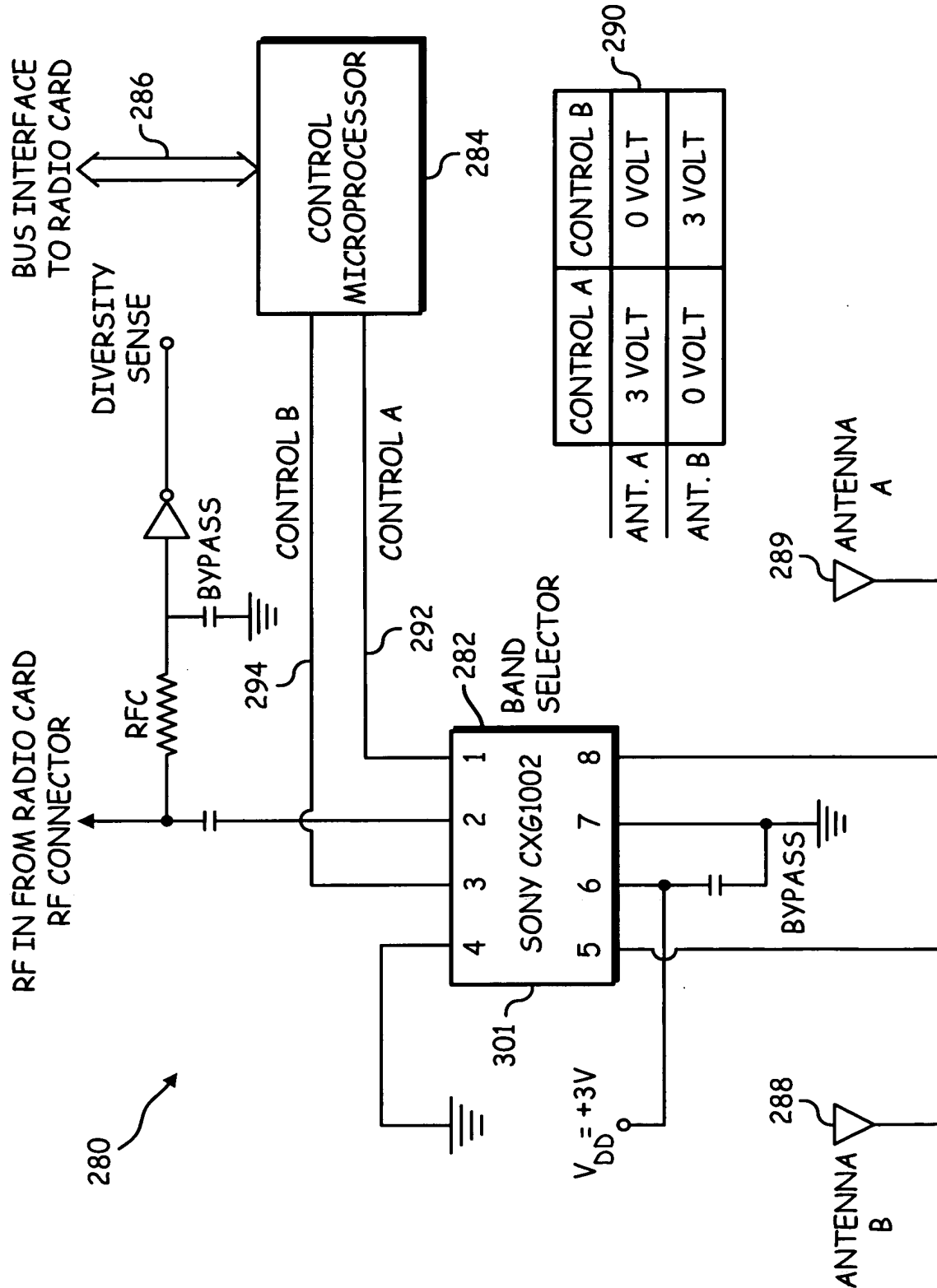


FIG. 29



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ANTENNA B WITH SELECTION DIVERSITY

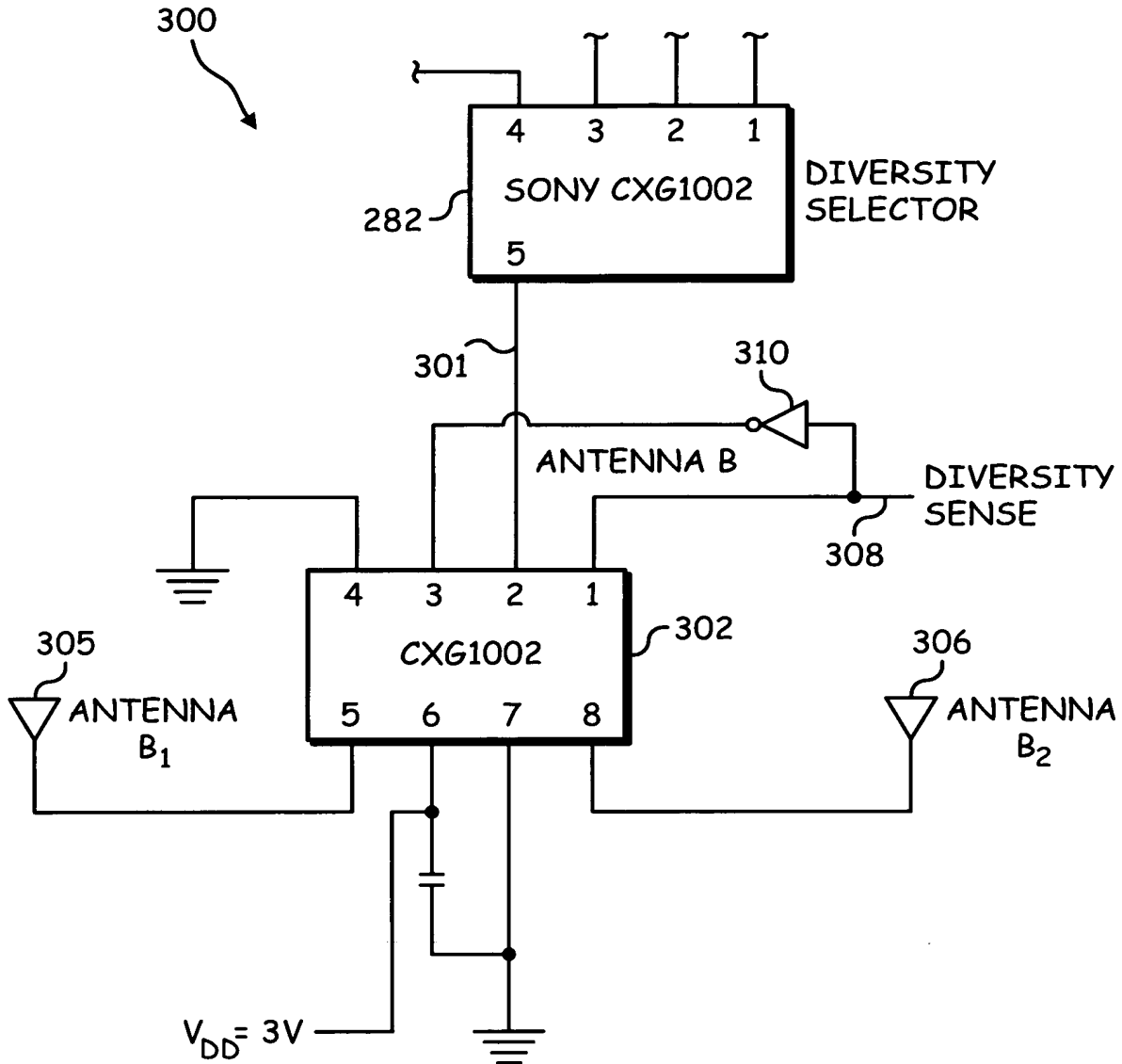


FIG. 30



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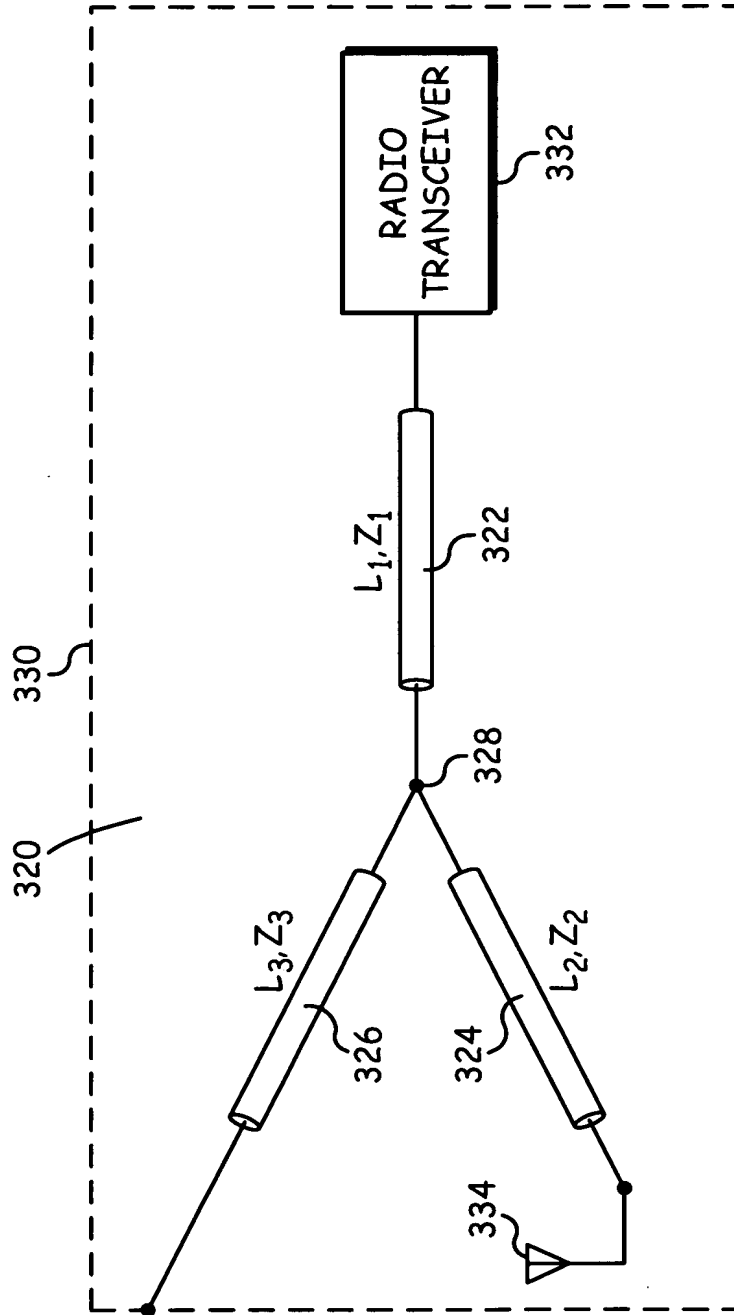


FIG. 31



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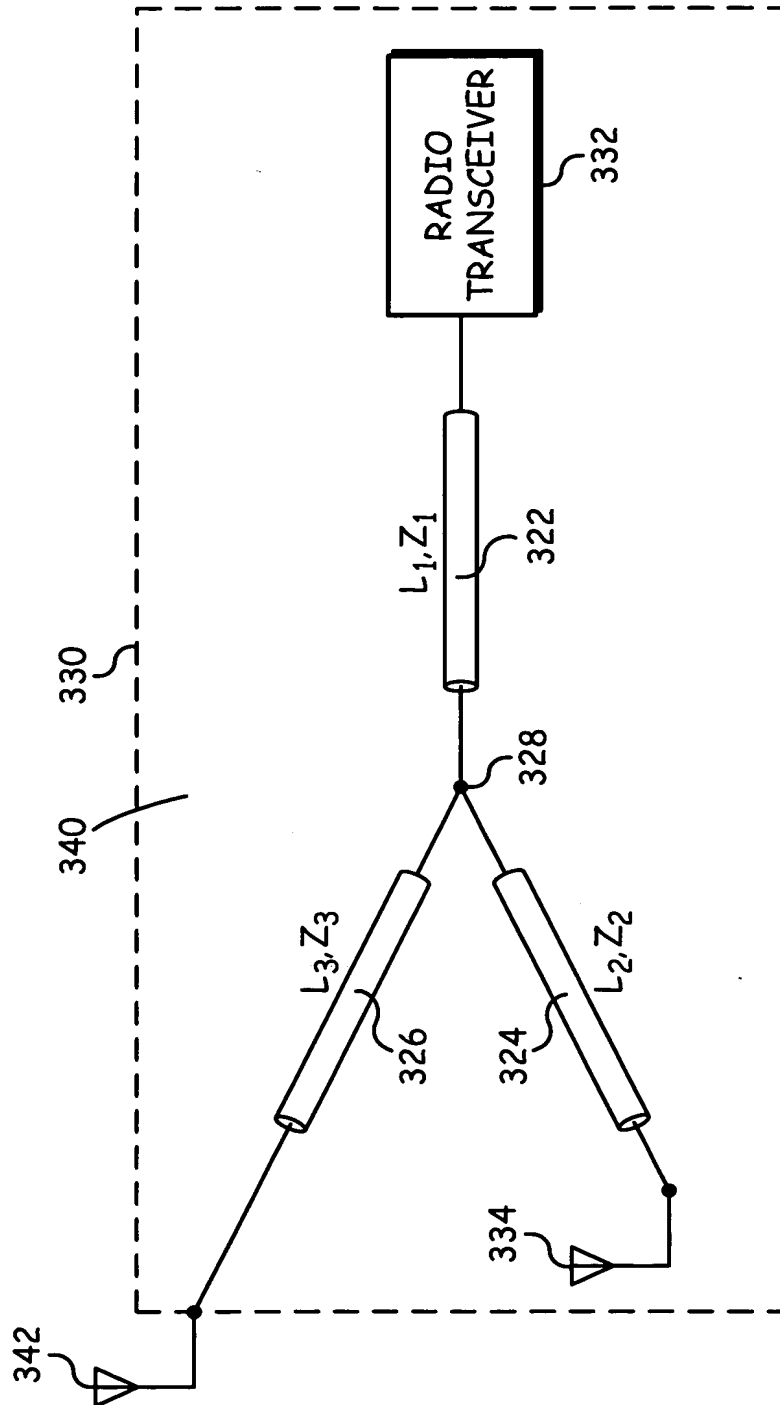


FIG. 32